AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph bridging pages 2 and 3 as follows:

A conventional example of the adaptive equalizer circuit is shown in Fig. 2. A sample value input 201 which is obtained by sampling reading signals 200 read by an optical disc not shown in the drawing by means of a sample hold circuit 205 is inputted to a system which is comprised of n pieces of unit delay elements D1-Dn which are connected with each other in the longitudinal direction. The unit delay elements D1-Dn have a time delay equal to a sampling period of the above-mentioned sample values and an output of one unit delay element becomes an input of one preceding sampling. In multiplication circuits MO-Mn, products of the signal 201 and the sample values outputted from respective delay elements and coefficients computed by coefficient control circuits CO-Cn are computed and the products are inputted into an addition circuit 203. An output from the addition circuit 203 is outputted as an output value 202 of the adaptive equalizer circuit and at the same time is inputted to a subtraction circuit 204. In the subtraction circuit 204, the difference between an output value Vo and an arbitrary given reference value is outputted as an adaptive error value. This reference value is determined such that the equalization characteristics of this adaptive equalizer circuit become the targeted transmission characteristics. ~~In this~~ This determination method is explained later in detail. The error value obtained by the subtraction circuit 204 is inputted to the coefficient control circuits CO-Cn. Each coefficient control circuit is constituted by a multiplication circuit and an integration circuit. For example, in the coefficient control circuit CO, the product of the input sample value 201 and the above-mentioned error value is computed by the multiplication circuit LO and the obtained value is averaged out by the integration circuit SO and is outputted to the multiplication circuit MO as a coefficient.

Please amend the paragraph bridging pages 5 and 6 as follows:

Since the PID regions are discontinuously present in the disc, to take the synchronicity with the reference clock, a region which is called a VFO (Variable Frequency Oscillator) section and in which signals of a single frequency are recorded is present. When the updating of the coefficients is performed using only the output values in the vicinity of the zero crossing point with respect to the waveforms regenerated in this VFO section, as shown in Fig. 5, with respect to the waveforms which differ in the amplitude of the waveform ~~in synchronous~~ in synchronization with the data sampling period, the equalizer error computed from the data sampled in zero-crossing portions 501-505 all become 0. However, no control is performed in regions other than the zero-crossing points an innumerable number of waveforms which satisfy the above-mentioned characteristics exist as shown in Fig. 5. This implies that there exist an innumerable number of conversing points so that the characteristics of the adaptive equalizer circuit become unstable.

Please amend the paragraph bridging pages 7 and 8 as follows:

To cope with this phenomenon, it may be considered to provide a plurality of sets of ~~Vth~~ threshold value and positive and negative reference values. However, since the estimation of the signal cycle is impossible, it becomes necessary to hold the value of the adaptive equalization output by storing means such as a memory or the like and to set the reference values while measuring the signal cycle. Accordingly, a cumbersome processing for administrating the timing of coefficient updating and the storing means such as the memory or the like becomes necessary.

Please amend the first full paragraph on page 8 as follows:

To solve the above-mentioned problem, an adaptive equalizer circuit which adds given equalization characteristics to signals inputted through a transmission path and performs a control

such that an equalization error obtained by performing an arithmetic operation based on an obtained output and a given reference value is minimized thus obtaining equalization characteristics, the adaptive equalizer circuit of the present invention is constituted such that an arithmetic . operation is performed in ~~synchronous~~ synchronization with a signal having a phase different from the reference clock signal of the above-mentioned signal by a 1/2 clock cycle, and equalization characteristics are changed by computing an equalization error based on ~~a first output value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive and the above-mentioned given reference value~~ a first output value and the above-mentioned reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from negative to positive.

Please amend the paragraph bridging pages 8 and 9 as follows:

Further, in the above-mentioned constitution which changes the equalization characteristics, the equalization characteristics are changed based on ~~the first output value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative and the first reference value, and the equalization characteristics are changed based on the first output value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from negative to positive and the second reference value~~ the first output value and the first reference value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics are changed based on the first output value and the second reference value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from negative to positive.

Please amend the first full paragraph on page 9 as follows:

Further, in addition to the above-mentioned changing operation of the equalization characteristics of the adaptive equalizer circuit, the adaptive equalizer circuit is constituted such that the equalization characteristics is changed based on ~~the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative and the second reference value, and the equalization characteristics is changed based on the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive and the first reference value~~ the second reference value and the output value immediately before the sign of the output of the adaptive equalizer circuit is changed from positive to negative, and the equalization characteristics is changed based on the first reference value and output value immediately before the sign of the output of the adaptive equalizer circuit is changed from negative to positive.

Please amend the paragraph bridging pages 9 and 10 as follows:

Further, in the above-mentioned constitution which changes the equalization characteristics, the equalization characteristics are changed based on ~~the first output value after the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative or from negative to positive and the first reference value, and the equalization characteristics are changed based on the output value immediately before the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative or from negative to positive and the second reference value~~ the first output value and the first reference value after a sign of an output of the adaptive equalizer circuit is changed from positive to negative or from

negative to positive, and the equalization characteristics are changed based on the second reference value and the output value immediately before the sign of the output of the above-mentioned adaptive equalizer circuit is changed from positive to negative or negative to positive.

Please amend the second full paragraph on page 10 as follows:

Further, the above-mentioned adaptive equalizer circuit is constituted such that the adaptive equalizer circuit is operated to sample an input signal with a signal having a phase different from the reference clock signal which is in ~~synchronous~~ synchronization with the input signal by a 1/2 clock cycle, and the equalization characteristics is changed based on an output value of the adaptive equalizer circuit.

Please amend the third full paragraph on page 10 as follows:

Further, the above-mentioned adaptive equalizer circuit is operated to sample an input signal with a signal having a phase different from the reference clock signal which is in ~~synchronous~~ synchronization with the input signal by a 1/2 clock cycle, and the adaptive equalizer circuit computes an output value of the adaptive equalizer circuit which is in ~~synchronous~~ synchronization with a signal having a phase different from the reference clock signal by a 1/2 clock cycle by an interpolation and changes the equalization characteristics using the computed value.

Please amend the paragraph bridging pages 10 and 11 as follows:

Further, the adaptive equalizer circuit is constituted such that the above-mentioned reference values are changed corresponding to the change of threshold values at the time of ~~binarizing~~ digitizing the output of the above-mentioned adaptive equalizer circuit.

Please amend the paragraph bridging pages 13 and 14 as follows:

In these drawings, numeral 101 indicates a PLL circuit, numeral 102 indicates a 1/2 clock cycle delay circuit, numeral 103 indicates a zero-crossing sign judging circuit, numeral 105 indicates a changeover switch, numeral 106 indicates a changeover switch, numeral 108 indicates a changeover switch, DO - Dn indicate unit clock cycle delay circuits, Dn+1 indicate 12 unit clock cycle delay circuits, DCZ indicates a unit clock cycle delay circuit, MO - Mn indicate multiplication circuits, LO - Ln indicate multiplication circuits. SO - Sn indicate integration circuits. numeral 203 indicates an addition circuit. numeral 1302 indicates an addition circuit. numeral 204 indicates a subtraction circuit. numeral 205 indicates a sample hold circuit and numeral ~~1302~~ 1301 indicates a binarization circuit.

Please amend the paragraph bridging pages 16 and 17 as follows:

The coefficient updating operation of the adaptive equalizer circuit of this embodiment is explained hereinafter using Fig. 10. Fig. 10 shows data series obtained at an output 202 of the adaptive equalizer circuit shown in Fig. 9. At the output 202, the white-dote data series in Fig. 10 obtained with a 1/2 cycle delay relative to the reference clock as in the case of the embodiment 1 can be obtained. The obtained data series are inputted to a zero-crossing sign judging circuit 103 as in the case of the embodiment 1. In the zero-crossing sign judging circuit 103, the first data after the zero-crossing in the data series are extracted as the coefficient updating sample. In Fig. 10, the data 1001 - 1004 become coefficient updating samples. The extracted data are respectively subjected to the sign judgement. In the ~~sing~~ sign judgement, a changeover switch 106 is controlled based on a control signal 107s such that when the sign of the extracted data is positive, the positive first reference value {Vref1 > 0) is selected and when the sign of the extracted data is negative, the

negative second reference value {Vref2 < 0) is selected. In case of Fig. 9, the second reference value Vref2 is selected at the data 1001, 1003 and 16 the first reference value Vref1 is selected at the data 1002, 1004.

Please amend the paragraph bridging pages 18 and 19 as follows:

The coefficient updating operation of this adaptive equalizer circuit is explained hereinafter. In the same manner as the embodiment 2, output data 202 from an FIR filter which are computed based on data sampled with a timing signal DLCK are inputted to a zero-crossing sign judging circuit 103. As an example, the operation at the time that data ~~901~~ 1001 in Fig. 10 are extracted as the coefficient updating data after the zero-crossing in the same manner as the embodiment. 2 is explained. When the data ~~901~~ 1001 are extracted, the changeover switch 105 is selected to the white-dot side and the coefficient updating is performed. Here, although the sign of the data ~~901~~ 1001 is judged as negative, data ~~904~~ 1005 which precedes the data ~~901~~ 1001 by one clock cycle by means of a unit delay circuit DCZ is inputted to the subtraction circuit 204 which computes the equalization error. Since the sign of the data ~~904~~ 1005 is opposite to the sign of the data ~~901~~ 1001, as the reference value, the positive first of the reference value (Vref1) which has the sign opposite to the ~~sigh~~ sign of the data ~~901~~ 1001 is selected. The equalization error computed accordingly are inputted to coefficient control circuits CEO - CEn. Here, in respective coefficient control circuits CEO - CEn, it is necessary to update the coefficients based on input sample data which are used for computing the data ~~904~~ 1005 and the above-mentioned equalization error. Accordingly, data DDO which delays the input data by 1 clock cycle is used for computing the coefficients ~~CSO~~ C0s. The data DDO are equal to the input data used at the time of computing the data ~~904~~ 1005. To compute the coefficient ~~CSI~~ C1s, data DDI which delays the input data by 2 clock cycles is used. This data

DD1 are equal to the data which delays the input data at the time of computing the data ~~904~~ 1005 by 1 clock cycle. In the same manner, to compute the coefficient ~~CSn~~ CnS, data DD(n+l) which delays the input data by (n+l) clock cycles is used. Accordingly, the coefficient ~~CSn~~ CnS can be computed based on the n clock cycle delay data at the time of computing the data ~~904~~ 1005 and the previously-mentioned equalization error so that the proper coefficient updating computing can be performed based on the data ~~904~~ 1005. Subsequently, after one clock cycle, the data ~~901~~ 1001 is inputted to the subtraction circuit 204. In ~~synchronous~~ synchronization with this inputting, based on the control signal 107s, the changeover switch 106 is changed over to the negative second reference value (Vref2) side which has the same sign as the data ~~901~~ 1005. Here, while holding the changeover switch 105 to the white dot side, the coefficient updating is performed based on the data ~~901~~ 1001. The equalization error computed based on the data ~~901~~ 1001 and the second reference value is inputted to Here, while holding the changeover switch 105 the coefficient control circuits CEO - CEn. Here, the input sample data DDO - DDn inputted to respective coefficient control circuits CEO - CEn are turned into data delayed by one clock cycle compared to data at the time of computing data ~~904~~ 1001 and these data are equal to data used for computing the data ~~901~~ 1005. Accordingly, the proper coefficient updating using the data ~~901~~ 1001 can be performed.

Please amend the paragraph bridging pages 20 and 21 as follows:

Fig. 13 shows a circuit block diagram of an adaptive equalizer circuit of a fifth embodiment of the present invention. In the drawing, blocks having the identical functions as those of Fig. 11 are given same symbols and their explanation is omitted. In the drawing, numeral 130 indicates a ~~binarization~~ digitization circuit which ~~binarizes~~ digitizes the data series obtained at an output 201. In this circuit, a threshold value Vslth which is used at the time of ~~binarization~~ digitization is

outputted to an addition circuit 1303 as a signal 1302s. The threshold value Vsl th is added to a first reference value Vrefl and a second reference value Vref2 after selection. Due to such a constitution, it becomes possible to make the first reference value Vrefl and the second reference value Vref2 of Fig. 10 follow the displacement of the symmetry of the input signal of the adaptive equalizer circuit and hence, the stable equalization characteristics can be ensured.

Please amend the paragraph bridging pages 23 and 24 as follows:

According to the adaptive equalizer circuit of the present invention, the equalization characteristics of the adaptive equalizer circuit are updated using the equalization error computed based on the adaptive equalizer circuit output which is obtained in ~~synchronous~~ synchronization with the reference clock signal of the input signal obtained from the transmission system after the zero-crossing by the 1/2 clock cycle or before and after the zero-crossing by the 1/2 clock cycle and the reference value which is arbitrarily given. Accordingly, in the system in which the amplitude is fluctuated, the stable adaptive equalization operation can be realized without changing over the reference value for computing the equalization error based on the amplitude. Further, by interlocking the reference value with the threshold value of the binarization circuit which constitutes the rear stage of the equalizer circuit, the equalization characteristics which exhibit the stability to the displacement of the symmetry of the input signal can be realized.